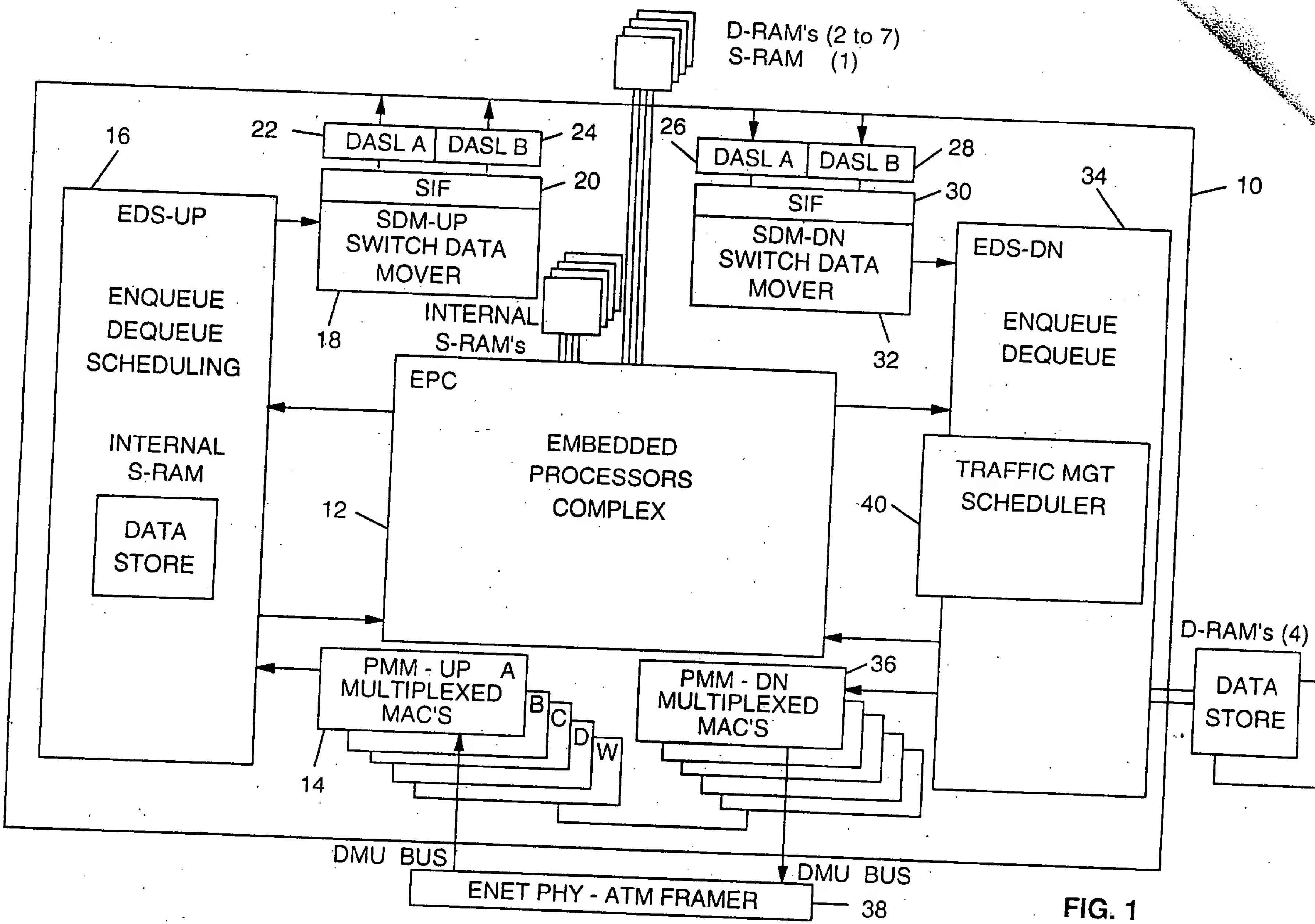

D-RAM's (2 to 7)
S-RAM (1)
10
16
EDS-UP
ENQUEUE
DEQUEUE
SCHEDULING
INTERNAL
S-RAM
DATA
STORE
22
DASL A
DASL B
24
20
SIF
SDM-UP
SWITCH DATA
MOVER
18
INTERNAL
S-RAM's
26
DASL A
DASL B
28
30
SIF
SDM-DN
SWITCH DATA
MOVER
32
34
EDS-DN
ENQUEUE
DEQUEUE
EPC
EMBEDDED
PROCESSORS
COMPLEX
12
40
TRAFFIC MGT
SCHEDULER
PMM - UP
MULTIPLEXED
MAC'S
A
B
C
D
W
14
36
PMM - DN
MULTIPLEXED
MAC'S
D-RAM's (4)
DATA
STORE
DMU BUS
DMU BUS
ENET PHY - ATM FRAMER
38

FIG. 1

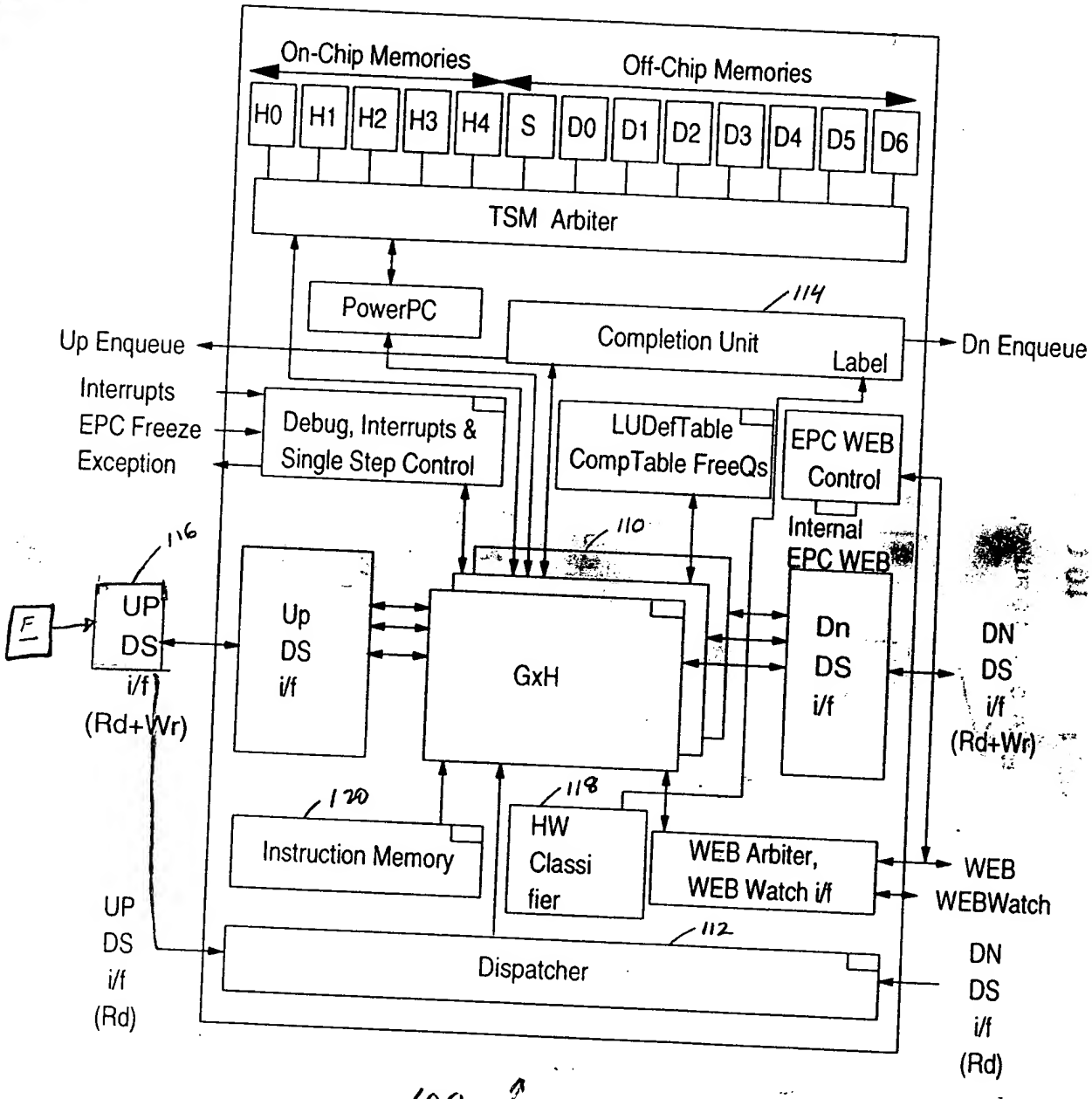


FIG. 2 BLOCK DIAGRAM OF THE EPC

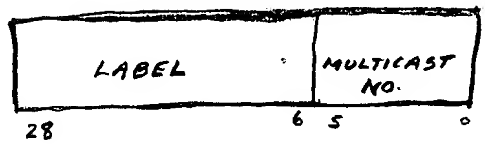
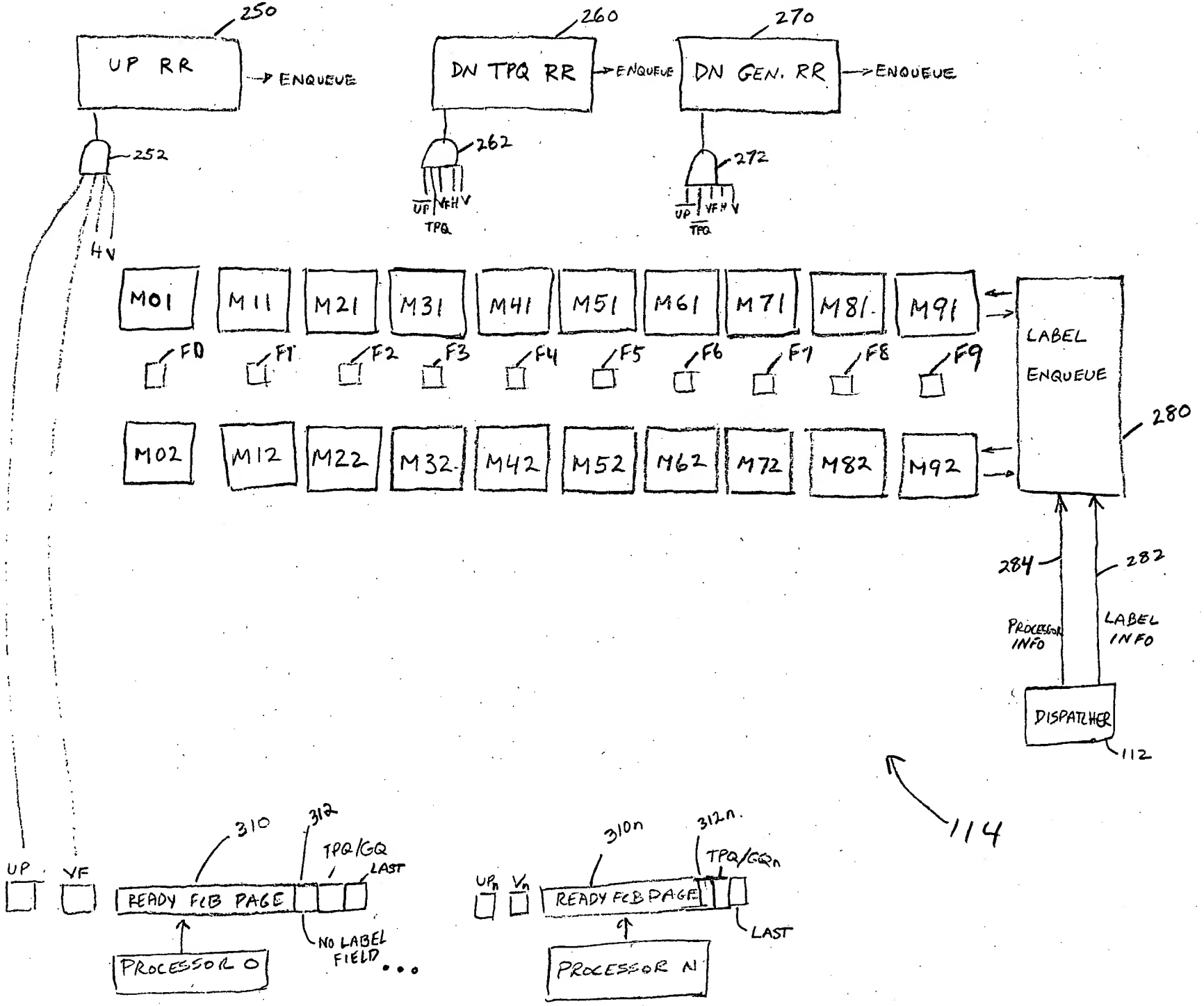


FIG. 3


250
UP RR
ENQUEUE
260
DN TPQ RR
ENQUEUE
270
DN GEN. RR
ENQUEUE
252
262
272
4V
UP
VF
TPQ
M01
M11
M21
M31
M41
M51
M61
M71
M81
M91
M02
M12
M22
M32
M42
M52
M62
M72
M82
M92
F0
F1
F2
F3
F4
F5
F6
F7
F8
F9
LABEL ENQUEUE
280
284
282
PROCESSOR INFO
LABEL INFO
DISPATCHER
112
114
310
312
TPQ/GQ
LAST
READY FCB PAGE
NO LABEL FIELD
PROCESSOR 0
310n
312n
TPQ/GQn
UPn
Vn
READY FCB PAGE
LAST
PROCESSOR N

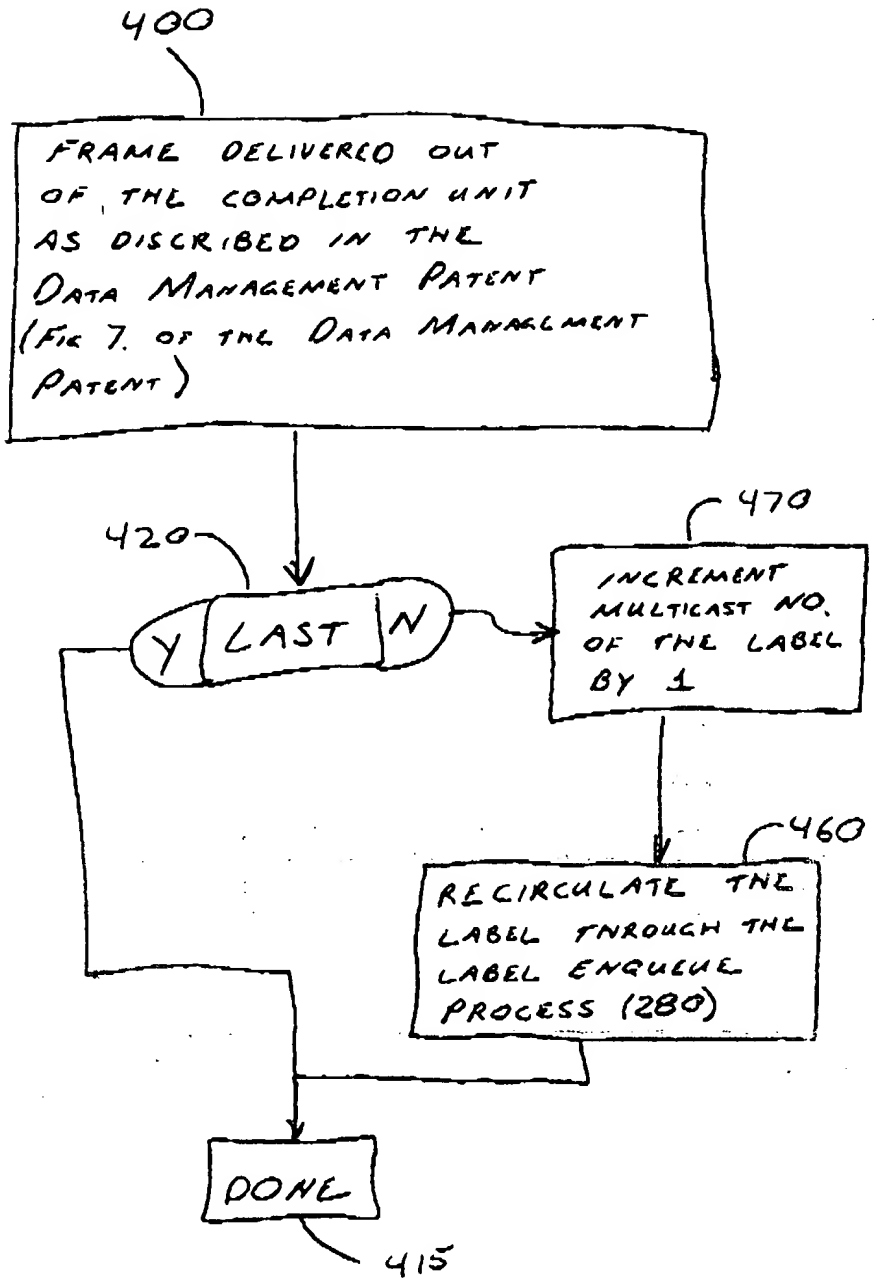

400
FRAME DELIVERED OUT OF THE COMPLETION UNIT AS DISCRIBED IN THE DATA MANAGEMENT PATENT (FIG 7. OF THE DATA MANAGEMENT PATENT)
420
Y
LAST
N
470
INCREMENT MULTICAST NO. OF THE LABEL BY 1
460
RECIRCULATE THE LABEL THROUGH THE LABEL ENQUEUE PROCESS (280)
DONE
415

FIG. 5

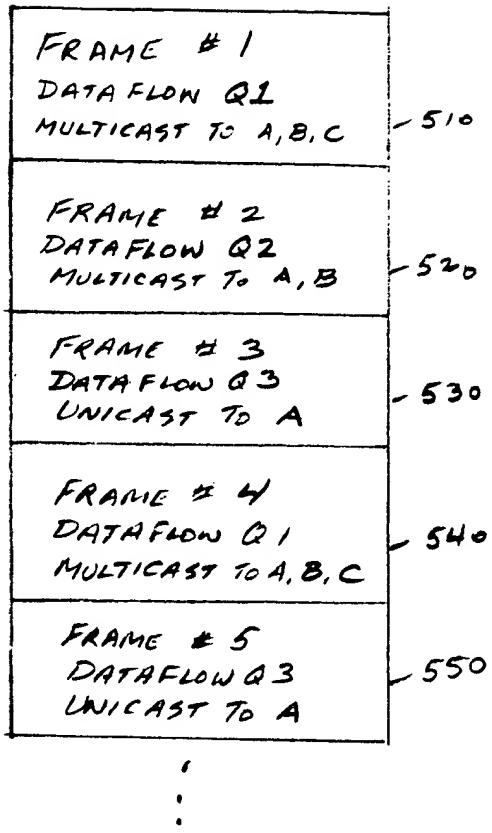


FIG. 6

FRAME	PROCESSOR	LABEL	DESTINATION	
1	0	Q1+0	A	701
1	0	Q1+1	B	702
2	7	Q2+0	A	703
3	5	Q3+0	A	704
4	2	Q1+0	A	705
2	7	Q2+1	B	706
4	2	Q1+1	B	707
1	0	Q1+2	C	708
4	2	Q1+2	C	709
5	4	Q3+0	A	710

FIG 7.